Listing of Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application. No claim has been cancelled, added, or amended.

1. (Previously presented) An amplification circuit, comprising:

an input to which an input voltage is provided,

a capacitor arrangement, and

a switching arrangement;

wherein:

the capacitor arrangement includes:

a first capacitor that is configured as a voltage-dependent capacitor having a first voltage-dependent capacitance, and

a second capacitor, coupled to the first capacitor, that is configured as a voltage-dependent capacitor having a second voltage-dependent capacitance;

the circuit is operable in two modes,

a first mode in which the input voltage is provided to an input terminal of at least the first capacitor, and

a second mode in which the switching arrangement causes charge to be redistributed between the first and second capacitors; and

the switching arrangement is configured to receive a first gain-control signal that is arranged to change the capacitance of the first capacitor and a second gain-control signal that is arranged to change the capacitance of the second capacitor.

2. (Previously presented) A circuit as claimed in claim 1, wherein the switching arrangement includes an input switch for selectively coupling the input voltage to the capacitor arrangement, and wherein in the first mode, the input switch couples the input voltage to the capacitor arrangement, and in the second mode, the input switch isolates the input voltage from the capacitor arrangement.

3. (Previously presented) A switch as claimed in claim 2, wherein in the second mode, at least one of the first and second gain-control signals change a voltage on a gain-control terminal of the first and/or second capacitor.

4. (Previously presented) A circuit as claimed in claim 3, wherein the change in voltage is on the gain-control terminal of the first capacitor and results in a reduction in the capacitance of the first capacitor.

5. (Previously presented) A circuit as claimed in claim 3, wherein the voltage on the gain-control terminal of each of the first and second capacitors is changed.

6. (Previously presented) A circuit as claimed in claim 5, wherein the change in voltage on the gain-control terminal of the second capacitor results in a reduction in the capacitance.

7. (Previously presented) A circuit as claimed in claim 5, wherein the voltage on the gain-control terminal of the first capacitor is increased and the voltage on the gain-control terminal of the second capacitor is decreased.

8. (Previously presented) A circuit as claimed in claim 7, wherein the voltage on the gain-control terminal of the first capacitor is increased from below the input voltage to above the input voltage, and the voltage on the gain-control terminal of the second capacitor is decreased from above the input voltage to below the input voltage.

9. (Previously presented) A circuit as claimed in claim 3, wherein the input switch is controlled by the voltage on the gain-control terminal of the first capacitor.

10. (Previously presented) A circuit as claimed in claim 9, wherein the input switch includes a first transistor with a gate connected to the gain-control terminal of the first capacitor.

11. (Previously presented) A circuit as claimed in claim 10, wherein in the second mode, a voltage on the gain-control terminal of the second capacitor is also changed, and wherein the input switch includes a second transistor in parallel with the first transistor, with a gate of the second transistor connected to the gain-control terminal of the second capacitor.

12. (Previously presented) A circuit as claimed in claim 1, wherein the input terminal corresponds to the gain-control terminal of each of the first and second capacitors, the switching arrangement includes: a first switch or switches coupling the input voltage to the gain-control terminal of the first and second capacitors; second switches coupling the respective gain-control signals to the gain-control terminals of the first and second capacitors; and an input switch coupling a reference voltage to other terminals of the first and second capacitors.

13. (Previously presented) A circuit as claimed in claim 12, wherein in the first mode, the first switch or switches and the input switch are closed, so that a voltage across the capacitors is dependent on the input voltage, and in the second mode, the second switches are closed and the output voltage comprises the voltage on the other terminals of the first and second capacitors.

14. (Original) A circuit as claimed in claim 12, wherein the first capacitor comprises a depletion n-type MOS device.

15. (Original) A circuit as claimed in claim 14, wherein the first and second capacitors comprise depletion n-type MOS devices.

16. (Previously presented) A circuit as claimed in claim 1, wherein the input is connected to the input terminal of the first and second capacitors, and the respective gain-control voltages are coupled to the gain-control terminals of the first and second capacitors through respective control switches of the switching arrangement.

17. (Previously presented) A circuit as claimed in claim 16, wherein the switching arrangement includes a shorting switch connected between the gain-control terminals of the first and second capacitors.

18. (Previously presented) A circuit as claimed in claim 17, wherein in the first mode, the control switches are closed and the voltages across the capacitors is dependent on the input voltage, and in the second mode, the shorting switch is closed and the output voltage comprises the voltage on the gain-control terminals of the first and second capacitors.

19. (Previously presented) A circuit as claimed in claim 1, wherein at least one of the first and second capacitors includes a transistor with source and drain connected together, and wherein one of the input terminal and gain-control terminal is defined by the gate and an other of the input and gain-control terminal is defined by the connected source and drain.

20. (Previously presented) A circuit as claimed in claim 19, wherein the transistor of the at least one capacitor comprises a thin film MOS transistor.

21. (Previously presented) An active matrix device comprising an array of device elements and circuitry for generating control signals for controlling the device elements, further comprising a circuit as claimed in claim 1 for increasing a voltage level of the control signals before supply to the device elements.

22. (Original) A device as claimed in claim 21, further comprising a latch circuit at the output of the amplification circuit.

23. (Previously presented) An active matrix display device comprising an array of display pixels, each display element having pixel refresh circuitry comprising an amplification circuit as claimed in claim 1 for amplifying a gate voltage of a control transistor within the refresh circuitry.

24. (Original) A device as claimed in claim 23, wherein the refresh circuitry comprises sensing circuitry for storing a display pixel voltage on a storage capacitor arrangement and writing circuitry for providing a voltage to the display pixel in dependence on the stored display pixel voltage, wherein the writing circuitry comprises the control transistor the gate voltage of the control transistor being provided by the storage capacitor arrangement and wherein the storage capacitor arrangement comprises the capacitor arrangement of the amplification circuit.

25. (Original) An active matrix array device comprising an array of device elements, each device element in the array being provided with a circuit as claimed in claim 1.

26. (Original) A device as claimed in claim 25, wherein the device elements comprise memory cells, image sensing pixels, or display pixels.

27. (Previously presented) A method of amplifying a signal, comprising:

providing an input signal to a capacitor arrangement comprising a first capacitor that has a voltage-dependent capacitance and a second capacitor that has a voltage-dependent capacitance;

causing charge to be redistributed between the first and second capacitors; ;

providing a first gain-control signal to change the capacitance of the first capacitor and a second gain-control signal to change the capacitance of the second capacitor; and

providing an output voltage dependent on the resulting voltage across the first capacitor.